Kevin Fronczak

Analog Architecture and Design

Redacted contact info due to spam. Reach out on LinkedIn if you'd like to get in contact:
https://www.linkedin.com/in/kfronczak/

PROFESSIONAL

ams AG - Image Sensor Solutions Division Rochester, NY

Sr. Staff Analog Design Engineer *August 2020 - Present*

- Analog Team Lead and IC Architect for global shutter Image Sensor devices primarily targeting consumer markets

Sony Electronics Inc. Rochester, NY

Staff Mixed Signal IC Design Engineer *July 2018 - July 2020*

- Work involves frequent communication with worldwide cross-functional teams, as well as mentoring of other analog engineers
- Involved in the Dynamic Frequency and Voltage Scaling (DFVS) power management architecture for next-gen stacked-chip CMOS image sensors in 40nm
    - Architected and designed a 5-uW unconditionally-stable external capacitorless LDO supporting up to 10mA of load current
    - Implemented an innovative scheme to handle undershoot during voltage-domain crossover in DFVS mode (to be patented)
- Led a small team in the evaluation of external delta-sigma-based temperature sensor IP for propagation within other global business units
- Responsible for the design of circuits to interface with a pixel array for a stacked-chip low-power CMOS imaging product in 40nm
    - Used unique multiplexing scheme to be able to intelligently bin adjacent columns for power reduction during motion detection capture

Synaptics Inc. Rochester, NY

Sr. Mixed Signal IC Design Engineer *February 2014 - July 2018*

- Helped lead introduction of a direct-conversion, delta-sigma based AFE in a 55nm node targeted for low power fingerprint sensing on mobile phones. Architecture achieved 50% cost reduction over existing solutions for no loss in performance
    - Transistor-level design of a low-noise current conveyor with innovative HF mixing topology meant to improve SNR with minimal overhead (US 10,606,386)
    - Performed interference susceptibility analysis on existing and proposed architectures and designed an innovative interference mitigation technique that took advantage of existing system design for improved performance (US 10,394,386)
- Architected, and implemented a prototype sub-uW power management architecture for next-generation capacitive sensors to aid in >30% power reduction over existing solutions (55nm)
    - Led this effort from proposal phase through silicon bring-up
    - Work involved brand-new designs for bias generation circuits, oscillators, and long sample-and-hold bandgap references (>1ms hold time)
    - Designed a nW-level time-to-digital (TDC) temperature sensor capable of sub-1℃ resolution as measured in silicon
- Designed subsystems for first market introduction of Touch and Display Driver Integrated Circuits (TDDI). Initial prototypes in 130nm, mass-produced parts in 55nm.

Synaptics Inc. Rochester, NY

Analog Design and Silicon Validation Contractor *June 2013 - February 2014*

- Performed extensive verification and validation on LDOs, VCOM drivers, LCD level shifters, and MIPI DSI

EDUCATION

Rochester Institute of Technology Rochester, NY

M.S. and B.S. in Electrical Engineering, August 2013

Thesis *Stability Analysis of Switched DC-DC Boost Converters for Integrated Circuits*

- Investigated small-signal modeling and stability requirements for boost converters, as well as a variety of OTA-based controller topologies, in order to aid in the measurement of boost converter stability on multiple ASICs. Also investigated the use of optimization algorithms as a way to improve controller design.

PATENTS AND PUBLICATIONS

- US 9,780,736 - Temperature compensated offset cancellation for high-speed amplifiers - Grant Oct. 3, 2017
  - Authors: Kevin Fronczak, Murat Ozbas, Yongang Chen
- US 9,817,428 - Current-mode Bandgap Reference - Grant Nov. 14, 2017
  - Authors: Kevin Fronczak, Eric Bohannon
- US 10,394,386 - Interference Detection - Grant Aug. 27, 2019
  - Authors: Kevin Fronczak, Eric Bohannon
- US 10,530,296 - Oscillator Temperature Coefficient Adjustment - Grant Jan. 7, 2020
  - Authors: Andrew Jabrucki, Eric Bohannon, Kevin Fronczak
- US 10,606,386 - Mixer Circuit - Grant Mar. 31, 2020
  - Authors: Kevin Fronczak, Eric Bohannon
- US 10,659,025 - Adaptive Bias Circuit for Power Event Detection Comparator - Grant May. 19, 2020
  - Authors: Kevin Fronczak, Mark Pude