ROCHESTER INSTITTUE OF TECHNOLOGY

Analysis of Sub-threshold Conduction in MOSFETs

EE712: Advanced Field-Effect Devices

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Abstract – Sub-threshold conduction is an important consideration when dealing with modern devices, especially due to the trend towards increasingly smaller device sizes. Shorter channels have adverse effects on sub-threshold swing, affecting device operation in this region. Analog designers would like a smooth and accurate model in order to properly utilize this highly efficient operating region, while digital designers would prefer to understand methods to minimize channel conduction when a device is sub-threshold. This paper will review previously published works that discuss analytical models for different sub-threshold concerns, including short-channel effects and the effects due to barrier-lowering. Experimental data is also presented which verifies some of these selected models. Finally, areas for further research into this operating region will be presented.

I. Introduction

The sub-threshold regime of MOSFETs is of particular interest to both analog and digital designers. In this region of operation, colloquially known as weak-inversion, the ratio of transconductance to current is very high, making it a very efficient operating region [1]. However, due to the nature of a parameter known as sub-threshold swing, the dependence on gate-source biasing causes distortion and nonlinear gain [1]. Ideally, this swing should be at a minimum of $\phi_t ln(10)$ but is typically much larger due to many different effects occurring within the transistor.

The digital designer is concerned about the sub-threshold region for an entirely different reason. In digital circuitry, a device can be in two states: "on", or "off". In the "off" state, the applied V_{GS} is less than V_T which, incidentally, is the same condition for sub-threshold conduction. Circuits that are critically dependent on this condition can exhibit non-ideal

behavior in that there will be at least some finite amount of current flow in what should be a zero-current state [2], [3].

The following sections will deal with this sub-threshold regime and discuss the effects it has on device performance. There are many different topics that can be considered in weak-inversion including threshold voltage shifts, drain-induced barrier-lowering, non-uniform doping effects, and the effects due to multiple gates: all of which are covered under Section II.

Section III will cover selected experimental and theoretical comparison plots to help gauge a specific model's accuracy over various parameters. Section IV will discuss where these models perform well, where they falter, and how they could potentially be improved with further research. Section V will present the conclusions formulated after the in-depth discussion of sub-threshold behavior.

II. Theory

Sub-threshold conduction is characterized by a current flow in the case when $V_{GS} < V_T$. An important parameter when discussing sub-threshold conduction is called sub-threshold swing and is given by equation (1).

$$S = \left(\frac{\partial \log I_D}{\partial V_{GS}}\right)^{-1} \tag{1}$$

As Vandamme *et al.* note in their paper, drain current for an NMOS transistor in weak-inversion can be modeled by equation (2) where I_0 is given in equation (3) [1].

$$I_D = I_0 10^{V_{GS}/S} \tag{2}$$

$$I_0 = I_x 10^{-V_T/S} \tag{3}$$

Vandamme *et al.*, however, sought to define a new equation for I_0 based on drain leakage current. For this, they made the following assumptions:

i). Channels are both wide and long

ii). The substrate is uniformly doped

iii). V_{DS} is small

iv). There is no mobility degradation

v). There are no edge effects

Given these assumptions, equation (4) was derived where I_x' is a technology-dependent parameter, η is a constant whose value is 0.9, and S_{min} is the sub-threshold swing when V_{GS} is at the boundary between weak and moderate inversion.

$$I_0 = \frac{W}{L} I_x' \times 10^{-\eta V_T/S_{min}} \tag{4}$$

The issue with (4) is that the assumptions made to derive it ignore many crucial details, which will be outlined in the following sections.

A) Shifting Threshold Voltage

As channel-length is decreased, the threshold voltage changes as a function of the length itself and V_{DS} [2]. In Taylor's analysis, he derived the following equation:

$$V_T = V_{FB} + 2\phi_F + \frac{qN_A}{2C_{ox}}\sqrt{K(2\phi_F + V_{BS})}\left\{1 + \frac{L - \sqrt{K(V_{bi} + V_{DS} + V_{BS})} - \sqrt{K(V_{bi} + V_{BS})}}{L - \sqrt{K(V_{bi} - 2\phi_F)} - \sqrt{K(V_{bi} + V_{DS} - 2\phi_F)}}\right\} \tag{5}$$

This is obviously quite a complex equation with many parametric dependencies. Note that here K is a constant equal to $\frac{2\epsilon_S}{qN_A}$. In order to simplify this sub-threshold analysis, let us first consider

the case where no bias is applied to the drain and where $V_{bi} = 2\phi_F$. This simplification yields equation (6) which is noticeably more compact than the previous threshold expression.

$$V_T = V_{FB} + 2\phi_F + \frac{qN_AL}{4C_{ox}} \tag{6}$$

In this new equation, where drain voltage is effectively ignored, there exists only a dependence on channel length, oxide thickness, and doping. These equations, as Taylor points out, work well for device lengths larger than 1 μm (refer to Figure 6 in Section III) but he does not extrapolate his data for anything smaller.

Fjeldly and Shur present equation (7) below for a threshold shift based on a concept known as charge-sharing where κ is a constant that accounts for this charge-sharing, and x_s and x_d are the depletion widths associated with the source and drain (respectively) [3].

$$\Delta V_T = -\frac{2\kappa W(x_s + x_d)\sqrt{\epsilon_s qN_A\phi_F}}{C_{ox}} \tag{7}$$

Essentially, the theory is that in short-channel devices the depletion region of the gate overlaps the depletion regions associated with both the drain and the source. This idea is illustrated in Figure 1 which was adapted from [3].

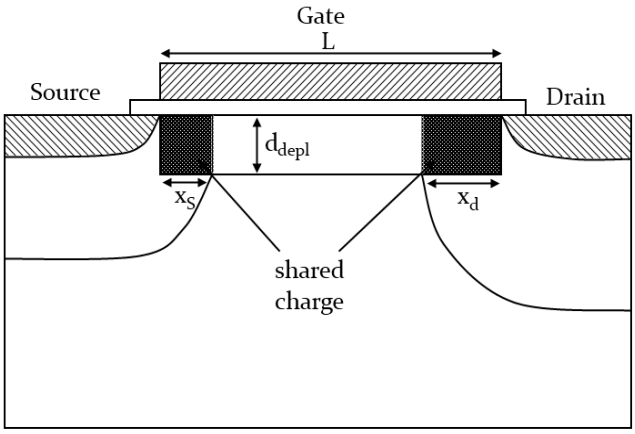

Figure 1. MOSFET cross-section with shared depletion zones illustrated. Adapted from [3].

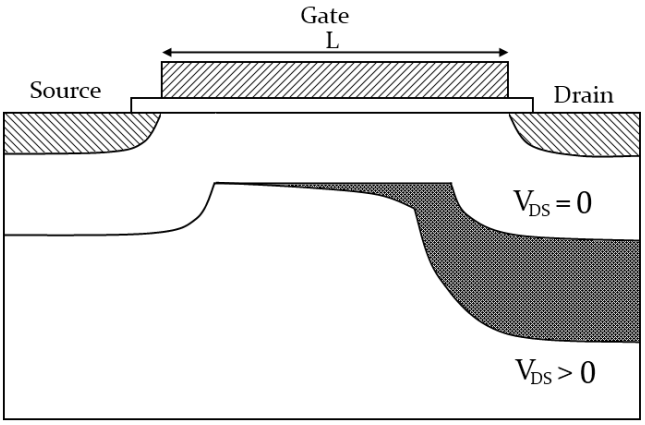

Figure 2. MOSFET cross-section with drain bias applied. Adapted from [3].

Fjeldly and Shur, however, note that this concept of charge sharing, which is assumed to be symmetric, begins to falter when a bias is applied to the drain. As V_{DS} is increased, the depletion region associated with the drain becomes larger and, as can be seen in Figure 2, the depletion charge is no longer symmetric. The threshold voltage will now be dependent on the applied bias V_{DS} [3]. It is here where the effects of drain-induced barrier-lowering (DIBL) begin to take hold.

In order to account for DIBL within the threshold voltage model, Fjeldly and Shur present the following equation:

$$\Delta V_T = -\frac{2\eta\chi d_{dep}^0}{\lambda}\frac{\sinh\left(\frac{x_s}{\lambda}\right)\cdot V_{DS}}{\cosh\left(\frac{L-x_s}{\lambda}\right)-\cosh\left(\frac{x_s}{\lambda}\right)} \tag{8}$$

Here, χ is a fitting parameter, d^0_{dep} is the depletion depth at V_{DS} of zero, and η is an ideality factor (the expression for λ can be found in the Appendix). As can be seen (8), the change in threshold voltage decreases exponentially as L is increased (this can be verified in Figure 7 in Section III). Likewise, the threshold shift changes linearly with an applied V_{DS}. There is an important limitation to this equation, however: if the drain voltage applied becomes high enough such that

the drain and source depletion regions overlap, the device will suffer from punch-through and (8) will diverge [3].

B) Drain-Induced Barrier Lowering (DIBL)

Taylor was able to achieve a sub-threshold current equation with DIBL effects taken into account, as shown below in (9).

$$I_{DS} = \frac{qW\bar{x}_d Dn_i exp\left(\frac{\psi_S - \phi_F}{\phi_t}\right)}{L - \sqrt{\frac{2\epsilon}{q\bar{N}_A}(V_{DS} + V_{bi} - \psi_S)} - \sqrt{\frac{2\epsilon}{q\bar{N}_A}(V_{bi} - \psi_S)} + 2\sqrt{\frac{\epsilon\phi_t}{q\bar{N}_A}}} \tag{9}$$

In order to achieve this model, a method was used in which the depletion regions were approximated to geometric shapes. Most notably, the depletion region under the gate is approximated to that of a trapezoid [2]. The regions that Taylor used can be seen in Figure 3. Taylor notes that as the depletion region under the drain (Region III in Figure 3) moves towards the source, the current becomes more dependent on drain voltage.

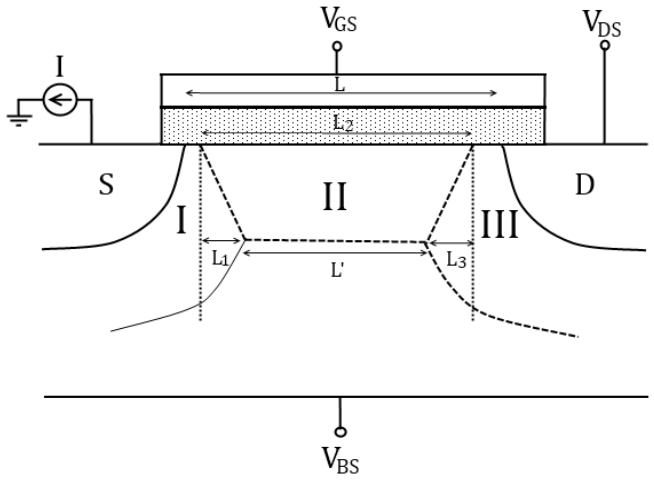

Figure 3. Geometric approximation for depletion regions. Adapted from [2].

There is, however, an issue with this approximation when dealing with DIBL: the depletion region potential near the edges is inaccurately estimated which, in turn, does not give an accurate estimate for the potential barrier near the source [4]. Since DIBL, by definition, is dependent on the potential barrier height, it follows to reason that any inaccurate estimate of this barrier would produce inaccurate estimates for current as well. Hence while (9) may be a good *approximation*, it does not accurately model the physical interactions in the channel due to the assumption that the potential at the surface is constant (which is only true for long-channel devices [5]).

To overcome this problem, Poole and Kwong treated the surface potential properly by noting that it will change as a function of the position in the channel [5]. The reason the sub-threshold current needs to be modeled this way is because in short-channel devices (where DIBL is of concern), the depletion regions occupy more area in the channel when compared to long-channel devices. The equation they present is shown below in (10). Since ψ_s is a function of the position in the channel (here, designated with x), the predicted current will be greater than that predicted in (9).

$$I_D = \frac{qWy_iDn_{p0}\left(1 - exp\left(\frac{-V_D}{\phi_t}\right)\right)}{\int_0^L exp\left(\frac{-\psi_S}{\phi_t}\right)dx} \tag{10}$$

C) Doping Effects

Both equations (9) and (10) reveal dependencies on doping and this, along with the fact that non-uniform doping profiles can modify the depletion width, has a direct effect on sub-threshold current [6]. Figure 4 depicts a plot of a MOSFET doping profile versus the distance from the interface.

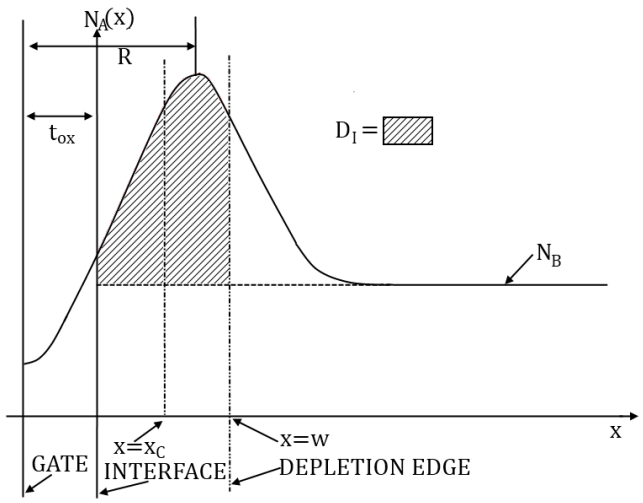

Figure 4. Doping profile versus distance from the interface. Adapted from [6].

This non-uniformity causes the number of implanted ions per area to become a function of the depletion width (as indicated by the shaded area in Figure 4) and results in a sub-threshold swing expression that depends on this relationship, as indicated by (11). Further parameter definitions can be found in the Appendix.

$$S = \phi_t \ln(10) \frac{1 + \frac{C_D}{C_{ox}}}{1 - \left(\frac{2}{a^2}\right)\left(\frac{C_D}{C_{ox}}\right)^2 (1+\gamma)^{-1}} \tag{11}$$

Brews notes that (11) is not applicable when implanted ions reside mainly in either the inversion layer or the interface, but that the occurrence of this is very rare due to the narrow nature of the inversion later [6]. The important result of (11) is that the sub-threshold swing primarily depends on the depletion capacitance to oxide capacitance ratio, or $\frac{C_D}{C_{ox}}$. Brews also notes that even though this analysis was carried out for long-channel devices, experiments suggest that the sub-threshold swing is not greatly influenced by short-channel effects as long as the device is sufficiently far away from punch-through [6].

D) Dual-Gate and FinFETs

Due to the proliferation of dual-gate MOSFETs, discussing their effects on sub-threshold conduction is important for a comprehensive analysis of this regime. Barsan attacked this problem by first realizing that a potential well or potential barrier can be created due to the addition of a second gate [7]. What happens is that either the current is controlled by the barrier, or the potential well acts as a drain. The ensuing result is that sub-threshold current is controlled by the highest potential barrier [7]. Figure 5 shows this barrier and well creation where (a) coincides with control by the first gate and (b) coincides with control by the second gate.

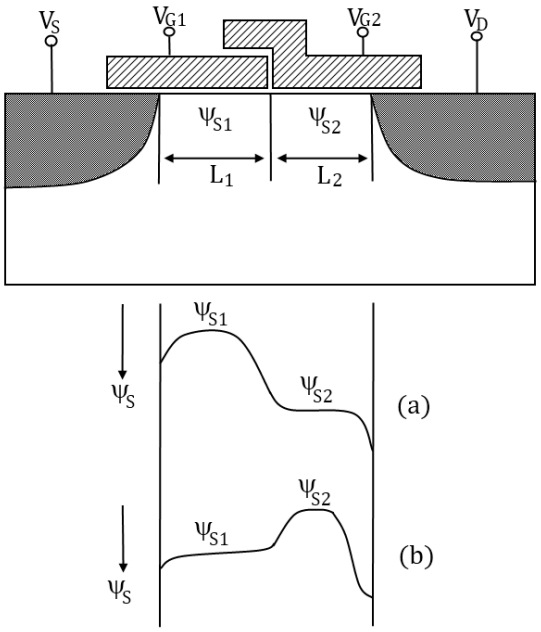

Figure 5. Dual-gate MOSFET cross-section with surface potential variation across channel. (a) $\psi_{s1} < \psi_{s2}$. *(b)* $\psi_{s1} > \psi_{s2}$. Adapted from [7].

For long-channel MOSFETs, Barsan presents (12) and (13) which predict the sub-threshold current taking into account both the channel lengths and surface potentials associated with the dual gate structure.

$$I_{ST} = \frac{W}{L_1} I_0 \frac{exp\left(-\frac{V_S}{\phi_t}\right) - exp\left(-\frac{V_D}{\phi_t}\right)}{\sqrt{\frac{\psi_{S1}}{\phi_t} - 1} \cdot exp\left(-\frac{\psi_{S1}}{\phi_t}\right) + \frac{L_2}{L_1}\sqrt{\frac{\psi_{S2}}{\phi_t} - 1} \cdot exp\left(-\frac{\psi_{S2}}{\phi_t}\right)} \tag{12}$$

$$I_0 = \mu \phi_t \sqrt{\frac{1}{2}\epsilon_s kT n_i} \cdot exp\left(-\frac{3}{2}\frac{\phi_F}{\phi_t}\right) \tag{13}$$

In (12), the familiar exponential dependence on V_{DS} exists in the dual-gate structure as does the dependence on channel width. The two quite obvious additions to the sub-threshold model are the dual values for both channel length and surface potential, as is expected. An interesting property of these equations is that since the surface potential is determined, in part, by the potential applied to the gate, for $\psi_{s1} << \psi_{s2}$, the sub-threshold current only depends on V_{G1}. Conversely, when $\psi_{s1} >> \psi_{s2}$, the sub-threshold current only depends on V_{G2} [7]. It follows, then, that if the two surface potentials are similar in magnitude that the current would then depend on both bias voltages.

As was the case with short-channel effects for a normal MOSFET, there are barrier-lowering effects in the dual-gate MOSFETs as well. However, instead of a drain-induced lowering, the barrier-lowering is actually induced by the *gates* [7]. As Barsan describes, both the potential under the first gate and the drain junction itself are capable of lowering the potential barrier under the second gate. Likewise, the barrier under the second gate is affected by both the first gate's potential and by the drain as well. However, calculating these effects is tricky due to their two-dimensional nature [7]. Thus, Barsan utilizes experimental parameters to help construct a model for short-channel dual-gate sub-threshold current shown below in (14) where I_0 is given in (13).

$$I_{ST} = \frac{W}{L_1} I_0 \frac{1 - exp\left(-\frac{V_{DS}}{\phi_t}\right)}{\sqrt{\frac{V_{SB} + \psi_{S1}}{\phi_t} - 1} \cdot exp\left(-\frac{\psi_{S1}}{\phi_t}\right) + \frac{L_2}{L_1}\sqrt{\frac{V_{SB} + \psi_{S2}}{\phi_t} - 1} \cdot exp\left(-\frac{\psi_{S2}}{\phi_t}\right)} \tag{14}$$

The short-channel (14) and long-channel (12) equations seem almost identical except for the inverse square-root dependence on the source-to-bulk potential V_{SB}; however, this is slightly misleading. Recall that in the short-channel case for dual-gate MOSFETs that the surface potential under either gate is dependent not only on its associated gate potential, but also the *second gate potential* and the *drain potential* due to gate-induced barrier-lowering [7]. This is shown below in (15) and (16) where $\alpha_{g1,2}$ are parameters dependent on $L_{1,2}$, V_{SB}, t_{ox}, and substrate doping. The expressions for $s_{1,2}$ and $\psi_{1,2}$ can be found in the Appendix.

$$\psi_{S1} = \frac{V_{G1S}}{s_1} + \frac{V_{G2S}}{s_2 \alpha_{g2}} + \frac{V_{DS}}{\alpha_{g2}\alpha_d} - \left(\psi_1 + \frac{\psi_2}{\alpha_{g2}}\right) \tag{15}$$

$$\psi_{S2} = \frac{V_{G2S}}{s_2} + \frac{V_{G1S}}{s_1 \alpha_{g1}} + \frac{V_{DS}}{\alpha_d} - \left(\psi_2 + \frac{\psi_1}{\alpha_{g1}}\right) \tag{16}$$

These expressions, however, differ from other multi-gate structures such as the FinFET. In order to properly analyze the sub-threshold swing, a solution needs to be obtained for electrostatic potential in all three dimensions [8]. El Hamid *et al.* were able to derive an equation for the sub-threshold swing that utilizes the summation of the eigenvalues of the 3-D electrostatic potential solution, shown in (17) and (18). The analytical limitation is that only undoped FinFETs were considered due to their higher mobility than that of doped devices [8].

$$S = \frac{\phi_t ln(10)}{1 - \sum_{\lambda_{z0,1}} \left[K_1 \cdot cos\left(\lambda_y y_c\right) \cdot cos(\lambda_z z_c) + K_2 \cdot cos\left(\lambda_y y_c\right) \cdot sin(\lambda_z z_c)\right]} \tag{17}$$

$$\lambda_x = \sqrt{\left(\frac{\lambda_z}{h_o}\right)^2 + \left(\frac{\lambda_y}{t_o}\right)^2} \tag{18}$$

Of note, the values λ_z and λ_y are the lowest eigenvalues in the potential solution. All other definitions can be found in the Appendix. Because the model takes into account the shifting nature of the conduction path within the channel due to the three-dimensional effects of the applied gate bias, this model compares admirably versus experimental data for all device dimensions as well as either a small or large value for V_{DS} [8]. Further experimental data is presented in Section III.

III. Experimental Results

Recall Taylor's analysis of the shifting threshold voltage in equation (5) with the approximation that the drain bias is zero in (6). Experimentally, these two equations are compared in Figure 6 and, as expected, are in good agreement for small values of V_{DS}. As can be seen, there is a discrepancy for the V_{DS} = 10 V case and that is caused by punch-through in the bulk.

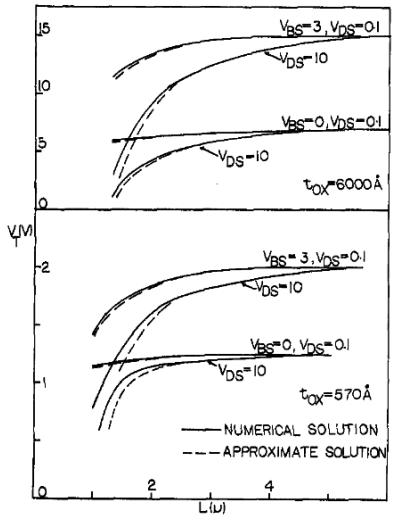

Figure 6. Threshold voltage with respect to channel length. N_A = 5.6 x 10 cm^{-3}, V_{FB} = 0. Taken from [2].

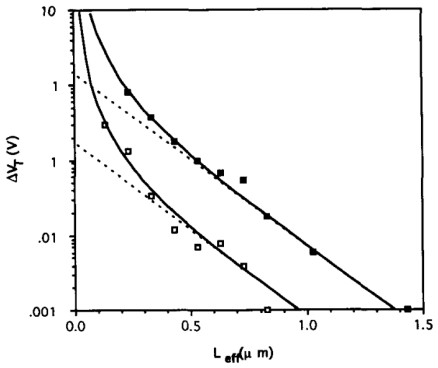

Figure 7. Experimental values (symbols), fitted calculations (solid line) and approximation (dotted line) for ΔV_T versus effective gate length. Top curve at 85 K, Bottom curve at 300 K. Taken from [3].

In a similar fashion, Fjeldly and Shur's model, (8), performed very well against experimental data, as seen in Figure 7, above. As long as the effective gate length is above 0.1 μm, they claim, this model is valid [3].

Taylor's model (9) for sub-threshold current is plotted against V_{GS} for varying values of drain voltage in Figure 8. The solid line corresponds to experimental results while the thinner line is the theoretical model. As can clearly be seen, the data fits very closely up until the point where $V_{GS} = V_T$ (which is expected since the model was derived with only sub-threshold considerations in mind).

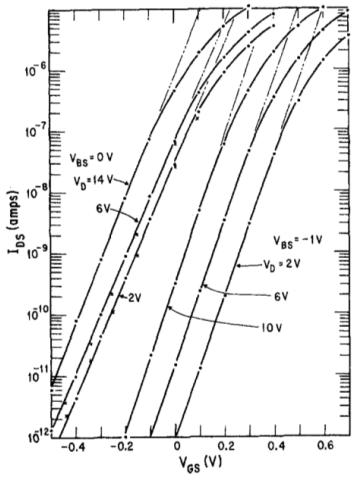

Figure 8. I_{DS} vs. V_{GS} for varying V_{DS} values for (9). Taken from [2].

The model (17) presented by El Hamid *et al.* shows very good correlation between itself and experimental data. The model was used for a fin height of 60 nm and plotted for a small V_{DS} value (in Figure 9a) and large V_{DS} value (in Figure 9b). Recall that El Hamid *et al*. claimed that despite the relocation of the conduction path for high values of V_{DS}, the model still accurately predicts sub-threshold swing [8]. This is corroborated with Figure 9b where the error between the model and experimental results is negligible up to larger values for the fin width. Despite the computational difficulty with (17) due to the 3-D electrostatic potential equation, this model is quite good at predicting the correct sub-threshold swing in modern devices.

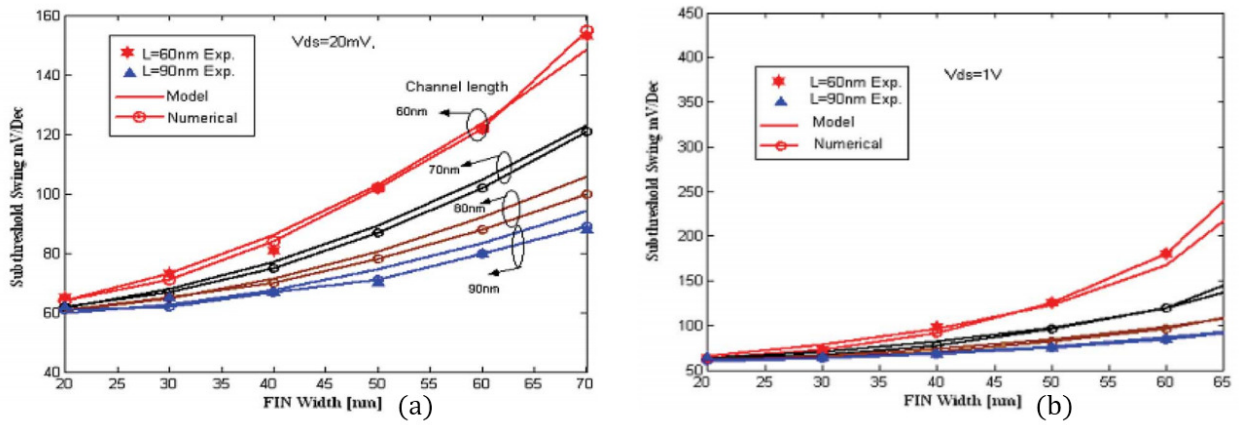

Figure 9. (a) Sub-threshold Swing for small V_{DS}. (b) Sub-threshold Swing for large V_{DS}. Taken from [8].

IV. Discussion

As presented in Section II, each model has its faults due to various approximations. Taylor's equations actually perform quite well and this is mainly attributable to the fact that both (5) and (9) take barrier-lowering effects into consideration. However, in this analysis Taylor assumed a uniform doping profile even though small variations in doping can largely impact the end result [2]. Another short-coming of the model, as Taylor points out, is that it does not take

into consideration any surface states. Any surface potential change due to trapped charges results in larger currents due to the exponential dependence on surface potential in (9).

In Section II, it was noted that Taylor only extrapolated his experimental and theoretical data out to 1 μm. Due to the relatively high accuracy of his model, it would be interesting to see the correlation at smaller, more modern, lengths. A likely result would be vast deviations in experimental and theoretical data due to the exacerbation of short-channel effects and increasingly more non-uniform doping profiles.

Fjeldly and Shur's threshold model in (8) exhibits excellent correlation with experimental data in Figure 7, as previously mentioned. The deviation at smaller effective gate lengths is due, in part, to the lack of consideration towards the contact junction depth. This depth, when coupled with the typical short-channel effects, can drastically alter the change in threshold voltage. [3].

The results shown in Figure 9 from El Hamid *et al.* only deviate at larger fin widths. This, unsurprisingly, is due to an approximation made with regard to the location of the conduction path. For (17), the conduction path parameter z_c (which corresponds to the path location normal to the surface) was set at a fixed value for simplicity. At larger V_{DS} values, however, this location begins to move closer and closer to the surface when the width is increased, resulting in the slight discrepancy show in Figure 9b.

The underlying assumption in all of El Hamid *et al.*'s analysis is that, as indicated in the paper title, it only deals with undoped finFETs. The explanation given in the paper is that undoped devices exhibit higher mobilities than that of doped devices; however no quantitative data was presented to verify the claim. It would certainly be a worth-while effort to investigate

the sub-threshold dependencies on doping in finFETs as a point for comparison. It is probable that the effects would be similar to that of a single-gate MOSFET, though the three-dimensional effects caused by non-uniformly doped substrates (as would likely be the case in modern devices) could have drastic adverse effects. This is certainly an area worth exploring further.

V. Conclusion

It is clear that there are a vast number of parameters that affect sub-threshold conduction. Since the condition for sub-threshold conduction is directly dependent on threshold voltage, it follows that lowering this value will decrease the range that the device will leak current. From a design standpoint, this can be done quite easily by simply decreasing the oxide thickness since, in both (5) and (7), there exists an inverse dependence on C_{ox}. The only other true design parameter available that helps alleviate sub-threshold conduction issues is the length of the device and, as every model presented predicts, decreasing the length will decrease the sub-threshold swing.

Short-channel effects are certainly the primary cause for concern in modern device sizes that are currently in the tens-of-nanometers range. The effects from barrier-lowering, trapped charge, and doping profiles (among others) are problematic from a design standpoint, since they cause irregularities in sub-threshold models, and from an analytical standpoint, since they're very complex to model. For devices that exhibit different behaviors in different dimensions, this complexity increases substantially. Understanding the underlying physics of whatever device a designer may be working with is paramount to minimizing adverse sub-threshold effects.

VI. References

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VII. Appendix

For equation (8):

$$\lambda = \frac{d_{dep}^0}{\sqrt{1 + \frac{\epsilon_i}{\epsilon_s}\frac{d_{dep}^0}{d_i}}} \tag{A.1}$$

For equation (11):

$$a = \frac{\sqrt{2} \cdot \epsilon_{sc} t_{ox}}{\epsilon_{ox} L_B} \tag{A.2}$$

$$\gamma = \frac{\sqrt{2}}{a}\frac{C_D}{C_{ox}}\left[m_0 - L_B\left(\frac{d\beta\phi_0}{dx}\right)_{x=w}\right] \tag{A.3}$$

$$\left(\frac{d\beta\phi_0}{dx}\right)_{x=w} = -\frac{1}{L_B^2} \cdot \int_w^\infty \frac{N_A(x_0) - p_0(x_0)}{N_B} dx_0 \tag{A.4}$$

For equations (15) and (16):

$$s_{1,2} = 1 + \sqrt{\frac{V_{01,2}}{2(V_{SB} + \overline{\psi_S})}} \tag{A.5}$$

$$\psi_{1,2} = \frac{2V_{SB} + \overline{\psi_S}}{1 + \sqrt{\frac{2(V_{SB} + \overline{\psi_S})}{V_{01,2}}}} + \frac{V_{FB1,2}}{s_{1,2}} \tag{A.6}$$

For equation (17):

$$K_1 = \frac{S_0}{\Delta R_0} \frac{D_0|_{x=x_{min}}}{\phi_{1-D}(y = y_c)} \tag{A.7}$$

$$K_2 = \frac{S_1}{\Delta R_1} \frac{D_0|_{x=x_{min}}}{\phi_{1-D}(y = y_c)} \tag{A.8}$$

$$S_0 = \frac{4}{\lambda_z^2} \cdot [sin(\lambda_z) - \lambda_z cos(\lambda_z)] \cdot cos\left(\frac{\lambda_z}{2}\right) \cdot \alpha_0|_{y=y_c} \tag{A.9}$$

$$S_1 = \left\{\frac{4}{\lambda_z} \cdot \left[sin(\lambda_z)\phi_{1-D}(y = y_c) - \alpha_1(y = y_c) \cdot \left(sin(\lambda_z)\left[\frac{1}{2} - \frac{1}{\lambda_z^2}\right] + \frac{cos(\lambda_z)}{\lambda_z}\right)\right] - V_t\right\} \cdot cos\left(\frac{\lambda_y}{2}\right) \tag{A.10}$$

$$\Delta R_0 = -\frac{sin(2\lambda_z) - 2\lambda_z}{2\lambda_z} \tag{A.11}$$

$$\Delta R_1 = \frac{sin(2\lambda_z) + 2\lambda_z}{2\lambda_z} \tag{A.12}$$

$$D_0 = \frac{sinh(\lambda_x \cdot x) - sinh(\lambda_x \cdot [x - L])}{sinh(\lambda_x \cdot L)} \tag{A.13}$$

$$\phi_{1-D}(y) = V_T \cdot ln\left[\frac{B_n^2}{2\delta} sec^2(B_n \cdot y)\right] \tag{A.14}$$

$$\delta = \frac{\epsilon_{si} \cdot t_0^2}{4qn_i V_T} \tag{A.15}$$